**Appl. No.** : 09/810,932
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IN THE SPECIFICATION:

**Please replace the paragraph appearing at page 13, line 8 to page 14, line 2 with the following:**

a1

It is contemplated that the various embodiments of the invention may be used to evaluate the characteristics of the first line 104, the second line 108, the third line 112, or lines 120 and 122 to thereby determine characteristics of the line, such as, but not limited to, the location of line anomalies that may effect data transmission. It is desired to obtain the highest data rate supportable by the lines 104, 108, 112, 120, 122 so that a maximum amount of data may be transferred in a minimum amount of time with the fewest number of errors. This enables more rapid upload, downloads, and greater and more reliable use of the lines 104, 108, 112, 120, 122. It is also contemplated that the invention may be practiced at any location in the communication system. In one preferred embodiment, the invention is integrated within modems at the communication interface 102, the C.O. switch 106, or the CPE 100. **[communication interface 102.]** The invention may also be used to determine line characteristics for each leg or path for symmetrical communication (identical or similar data transmission rates between devices) or asymmetrical communication (different data transmission rates between devices).

**Please replace the paragraph appearing at page 14, lines 3-8 with the following:**

a2

Figure 2A illustrates a block diagram of example configuration in relation to a communication line and an example line anomaly. A sequence generator and transmit module 200 connects to a hybrid 204. The hybrid 204 connects to channel 208. In one embodiment, the channel 208 comprises a twisted pair conductor. In another embodiment, the conductor

a2 End

comprises fiber optic cable. In yet another embodiment, the channel may comprise coaxial cable or radio waveguide.

**Please replace the paragraph appearing at page 23, line 9 to page 24, line 2 with the following:**

a3

Figure 4 illustrates a more detailed block diagram of an example embodiment of one configuration of the invention. Broadly, the elements of Figure 4 include **[includes]** a transmit module 400 and a receive module 404. Connecting the transmit module 400 and the receive module 404 is a line interface 408 and other possible logic and lines (not shown). The line interface 408 connects the transmit module 400 and the receive module 404 to a communication channel 412. The line interface 408 **[412]** includes an apparatus to separate or filter the transmitted signal from the received signal and attempts to impedance match the transmit module 400 to the channel 412 and the receive module 404 to the channel. In one embodiment, the line interface 408 comprises a hybrid. The line interface 408 may also be configured to interface a single conductor of the transmit module 400 or the receive module 404 to twisted pair conductors. Although designed to reduce impedance mismatch, the line interface 408 **[412]** often creates some mismatch, and hence may create a reflection during operation of the sequence time domain reflectometry as described herein. This reflection may be referred to near-end echo.

**Please replace the paragraph appearing at page 25, line 11 to page 26, line 2 with the following:**

a4

Figure 5 illustrates a block diagram of an example embodiment of a sequence generator configured using a linear feedback shift register or scrambler type implementation. An input 500 connects to a summing unit 504. All arithmetic operations may be performed in a modulo-2 fashion. The summing unit 504 has an output connected to an output line 508 and a delay register 510A. The output of the delay register 510A connects to a multiplier 514A, having a multiplier set to $C_1$, and to another delay register 510B. The output of delay register 510B connects to N number of other delay registers and multipliers as shown by connections 524 until connecting to a delay register 510C and to a multiplier 514B $C_{N-1}$. The output of delay register 510C connects to a multiplier 514C that has a multiplier $C_N$. One or more summing junctions 520A, 520B, 520C as shown combine the output from the multipliers. This creates an Nth order generator due to the N memory elements or delay registers 510. This thus generates an output based on the content of the registers, also known as the state of the scrambler. Thus, the total number of different possible states of the generator is $2^N$.

**Please replace the paragraph appearing at page 26, line 19 to page 27, line 7 with the following:**

a5

The output of the register 608 connects to multiplier 612B having a multiplier value $M_1$. The output of the multiplier 612B connects to the summing junction 624 to add the output of the multiplier 612B and the multiplier 612A. The output of the register 608 also connects to a register 616, the output of which connects to multiplier 612C. The output of the multiplier 612C

a5 End

connects to summing junction 636, which also receives the output of summing junction 624. The tap delayed line 600 continues in this configuration until connecting to a register 632 that has an output connected to a multiplier 612D with a multiplier factor $M_{2^N-1}$. The output of multiplier 612D connects to a summing junction 644 that also receives the output of the previous summing junction 636 to generate an output on output line 650.

**Please replace the paragraph appearing at page 30, line 19 to page 31, line 6 with the following:**

a6

Although numerous specific sequences are provided below, it is contemplated that any type sequence may be used. The text Introduction to Spread Spectrum Communications, **[Introduction to Spread Spectrum Communications]** written by Peterson, Ziemer and Borth, (Prentice Hall, 1995), which is incorporated herein in its entirety, provides a discussion on different sequences, and in particular, different types of M-sequences. Table 3-5, from the above-referenced text, provides a list of primitive polynomials that may be used to generate the sequence. Any sequence period may be selected. **[Other]** There exist sequence signals other than those listed that are contemplated for use with the invention**[, than those listed, also exist]**.

**Please replace the paragraph appearing at page 44, lines 6-12 with the following:**

a7

One example embodiment of an adaptive predictive response filter comprises a tapped delay line configuration as shown in Figure 6. The multiplier values M are the values of interest in the prediction filter 1004 **[1012]**. This may be implemented as a finite impulse response filter. The Electronic Handbook, **[The Electronic Handbook]** edited by Jerry C. Whitaker from CRC

a7 End

Press, Inc., 1996, which is incorporated in its entirety herein, contains a discussion of digital and adaptive filters at page 749-772. It is contemplated that a direct form structure or a module form structure may be used.

**Please replace the paragraph appearing at page 45, line 18 to page 46, line 14 with the following:**

a8

At a step 1214, the system monitors for and receives any reflection signals generated by the transmission of step 1212. The reflection signal may be defined as the overall signal(s) received during a period of time after the transmission of the original sequence signal over the channel. Thus, the reflection signal may actually comprise several periods of silence and several individual echoes created by the sequence signal encountering impedance mismatches or other anomalies as it travels down the channel. During receipt, the reflection is converted to a digital format at a step 1216. The signal may be stored or processing may continue at step 1220 by filtering the reflection signal to remove signals at unwanted frequencies. At step 1222, the system correlates the reflection signal with the original sequence signal. The correlation reveals the location of peaks within the reflection signal. Considered in different terminology, the channel is monitored after the transmission of the sequence signal for a period of time sufficient for any reflections generated by the transmission to be recorded by the monitoring. The received signals during this period of time are converted to the digital domain and stored or processed. Correlation occurs at step <u>1222</u> **[1220]** between the original sequence signal and any signals recorded during the monitoring period of step 1214. Peaks in the correlated signal occur at the points of time in the received signal when a reflection was received.

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**Please replace the paragraph appearing at page 47, line 18 to page 48, line 10 with the following:**

a9

Figure 14 illustrates an alternative method of sequence generation such as might be implemented for use with a table look-up method. At a step 1402, the channel analysis process is initiated. Thereafter at a step 1406, the operation specifies a sequence for generation. Once the desired sequence is <u>specified, at a step 1410</u> **[specified at a step 1410,]** the system obtains or is provided a memory address for the sequence data. Once the location in memory or the look-up table is provided or obtained, the system begins outputting the data items of the sequence. This occurs at step 1414. The operation then progresses to a step 1418, where the system queries to determine if there are additional data items remaining in the sequence. If additional data items exist, then the operation returns to step 1414 and an additional data item is output. If at step 1418 there are no more additional data items in the sequence to be output, then the operation progresses to a step 1422 to indicate that the sequence is complete and that the receiver aspects of the sequence time domain reflectometry should begin monitoring for reflection signals.

**Please replace the paragraph starting on page 53, line 15 to page 54, line 3 with the following:**

a10

At a step 1814, the peak in the near-end echo is assigned $T_1$ and referenced as time = 0. Thereafter, at a step 1818, the operation calculates, in relation to $T_1$, the time at which the next peak in the reflection signal occurs. This is assigned time $T_2$. At step 1822, the processing subtracts <u>$T_1$ from $T_2$</u> **[$T_2$ from $T_1$]** to determine the time <u>differential</u> it took between the sequence signal start and the first reflection. This time is assigned $T_{R1}$ for purposes of this discussion.

a10 End

Next, at step 1826, the process multiplies $T_{R1}$ by the velocity of propagation for the signal through the medium of the channel. This calculation yields a distance value, which reveals the location of the first line anomaly. At a step 1830, the operation repeats for the other peaks in the reflection signal.

**Please replace the Abstract appearing at page 75 with the following:**

a11

A method and system for performing sequence time domain reflectometry to determine the location of line anomalies in a communication channel is disclosed. In one embodiment, the system generates a sequence signal and transmits the sequence signal over a channel that is the subject of the sequence time domain reflectometry analysis. The system monitors for and receives one or more reflections, collectively a reflection signal, and presents the reflection signal to a reflection processing module. **[The module also has access to the original sequence signal that was transmitted over the channel. Various methods of processing the reflection signal are available to determine the location of the line anomalies.]** In one embodiment, the reflection signal is correlated with the original sequence signal to generate a correlated signal. The system may perform **[performs]** signal analysis on the correlated signal to determine a time value between the start of the reflection signal and the subsequent points of correlation. Based on the time value and the rate of propagation of the signals through the channel, the reflection processing module **[can determine]** determines a distance **[from the system]** to a line anomaly. **[In another embodiment, the original sequence signal is fed into a predictive filter and processed based on coefficient values of the predictive filter. The output of the predictive filter is compared to the reflection signal and the results of the comparison used to adjust**

a11 End



**the coefficients of the predictive filter. The reflection processing module adjusts the coefficients until the predictive filter output generally matches the reflection signal, at which point the coefficient values may be used to determine the distance from the system to a line anomaly.]**